Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An integrated circuit structure, comprising:
a substrate having a top surface defining a horizontal direction, said substrate of a first dopant type;
a first horizontal layer in said substrate, said first layer of a second dopant type; and
a second horizontal layer of said first dopant type, said second layer on top of said first layer and between said top surface of said substrate and said first layer, said second layer electrically modulated by said first layer.

[c2] 2. The structure of claim 1, further including:
a source and a drain of said first dopant type in said second layer and a gate formed on said top surface and aligned to said source and said drain; and
a first vertical bipolar transistor comprising said source, said second layer and said first layer; and
a second vertical bipolar transistor comprising said drain, said second layer and said first layer.

[c3] 3. The structure of claim 2, further including
a third horizontal layer of said second dopant type on top of and in contact with said first layer and extending vertically into said first layer, said second layer further

electrically modulated by said third layer.

[c4] 4. The structure of claim 3, wherein said third layer extends horizontally under said source, said drain and said gate.

[c5] 5. The structure of claim 3, wherein said third layer extends horizontally under a shallow trench isolation formed between said source or said drain and a contact to said second layer.

[c6] 6. The structure of claim 3, wherein said third layer extends horizontally under a contact to said second layer.

[c7] 7. The structure of claim 2 further including:
vertical isolation comprising shallow trench isolation in combination with deep trench isolation, trench isolation or diffused isolation;
said vertical isolation extending vertically from said top surface of said substrate into or past said first layer and isolating said second layer.

[c8] 8. The structure of claim 1, further including:
multiple fingers of source, multiple fingers of drain or multiple fingers of both source and drain a gate formed on said top surface and aligned to said source and drain fingers;
one or more vertical bipolar transistors each comprising

one source finger, said second layer and said first layer; and

one or more vertical bipolar transistors each comprising one drain finger, said second layer and said first layer.

[c9] 9. The structure of claim 1, wherein said first horizontal layer is the same as a subcollector of a bipolar transistor formed in said substrate.

[c10] 10. The structure of claim 1 wherein said first dopant type is P-type and said second dopant type is N-type.

[c11] 11. The structure of claim 1, wherein said second layer comprises epitaxial silicon.12.A trigger device comprising:

a lateral MOSFET comprising a source, a drain, a gate and a body;

a modulating layer under and in contact with said body;

a first vertical bipolar transistor comprising said source, said body and said modulating layer; and

a second vertical bipolar transistor comprising said drain, said body and said modulating layer.

[c12] 12.A trigger device comprising:

a lateral MOSFET comprising a source, a drain, a gate and a body;

a modulating layer under and in contact with said body;

a first vertical bipolar transistor comprising said source, said body and said modulating layer; and
a second vertical bipolar transistor comprising said drain, said body and said modulating layer.

[c13] 13. The trigger device of claim 12, further including means for lateral isolation of said source, said drain and said body.

[c14] 14. The trigger device of claim 12, further including a modulator extension, in electrical contact with and extending vertically from said modulator into said body.

[c15] 15. The trigger device of claim 12, wherein said source, said drain or both said source and said drain comprise multiple fingers and said first vertical bipolar transistor, said second vertical bipolar transistor or both said first and second vertical bipolar transistors comprise multiple bipolar transistors, one vertical bipolar transistor for each source finger and one vertical bipolar transistor for each drain finger.

[c16] 16. The trigger device of claim 12, wherein application of a bias to said modulator decreases a gate voltage at which MOSFET breakdown occurs.17. A method of electrostatic discharge protection, comprising:
providing trigger device comprising:

a MOSFET having a source, a drain, a gate and a body in a substrate;
a modulator under and in contact with said body;
a first vertical bipolar transistor comprising said source, body and modulator; and
a second vertical bipolar transistor comprising said drain, body and modulator;
coupling said modulator to said substrate and to an I/O pad; and
coupling said modulator and said drain to an input gate, to a double gated diode pair and input gate network or to a clamping network.

[c17] 17. A method of electrostatic discharge protection, comprising:
providing trigger device comprising:
a MOSFET having a source, a drain, a gate and a body in a substrate;
a modulator under and in contact with said body;
a first vertical bipolar transistor comprising said source, body and modulator; and
a second vertical bipolar transistor comprising said drain, body and modulator;
coupling said modulator to said substrate and to an I/O pad; and
coupling said modulator and said drain to an input gate,

to a double gated diode pair and input gate network or to a clamping network.

[c18] 18. The method of claim 18, further including, applying a bias voltage to said modulator to change the forward biases on said first and second vertical bipolar transistors.

[c19] 19. The method claim 17, further including, applying a bias voltage to said modulator to change the lateral resistance of said body.

[c20] 20.The method of claim 17, further including coupling said gate and said source to ground.